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6	a gate electrode formed only on said first side of the silicon layer between the first
7	diffused region and the second diffused region interposing a gate insulating film between the gate
8	electrode and the silicon layer;
9	a contact electrode formed on said first side of the silicon layer and connected to the
10	second diffused region; and
11	a capacitor formed only on said first side of the silicon layer and having a storage
12	electrode connected to the first diffused region;
13	a bit line formed on said second side of the silicon layer and electrically connected to the
14 W	second diffused region via the contact electrode;
15 Ç	a support substrate formed on said first side of the silicon layer for supporting the device
16	layer interposing an insulating film between the support substrate and the device layer; and
17 💆	a strapping word line formed on said second side of the silicon layer and connected to the
16 H 17 D 18 D H	gate electrode.
1	30. (New) A semiconductor memory device comprising:
2	a device layer including:
3	a silicon layer having a first diffused region and a second diffused region formed
4	therein and having substantially flat surfaces, said silicon layer defining a first side and a second
5	side;

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6	a gate electrode formed only on said first side of the silicon layer between the first
7	diffused region and the second diffused region interposing a gate insulating film between the gate
8	electrode and the silicon layer;
9	a contact electrode formed on said first side of the silicon layer and connected to the
10	second diffused region; and
117	a capacitor formed only on said first side of the silicon layer and having a storage
12	electrode connected to the first diffused region;
12 H	a bit line formed on said second side of the silicon layer and electrically connected to the
14 💢	second diffused region via the contact electrode;
14 JJ 15 📮	a support substrate formed on said first side of the silicon layer for supporting the device
16	layer interposing an insulating film between the support substrate and the device layer; and
17 <u>D</u>	a strapping word line formed on said first side of the silicon layer and connected to the gate
16 H 17 C 18 C	electrode.
1	31. (New) A semiconductor memory device comprising:
2	a device layer including:
3	a silicon layer having a first diffused region and a second diffused region formed
4	therein and having substantially flat surfaces, said silicon layer defining a first side and a second
5	side;

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6	a gate electrode formed only on said first side of the silicon layer between the first
7	diffused region and the second diffused region interposing a gate insulating film between the gate
8	electrode and the silicon layer;
9	a contact electrode formed on said first side of the silicon layer and connected to the
10	second diffused region; and
11	a capacitor formed only on said first side of the silicon layer and having a storage
12	ectrode connected to the first diffused region;
13	a bit line formed on said second side of the silicon layer and electrically connected to the
14	second diffused region via the contact electrode;
15	a support substrate formed on said first side of the silicon layer for supporting the device
16	layer interposing an insulating film between the support substrate and the device layer; and
17 N	a shield electrode formed above the bit line for suppressing interference between the bit lines.
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